Amendments to the Specification:

Please replace the paragraph starting on page 8, line 1 with the following:

~~A~~ The clock recovery block 108 receives this rough clock signal and uses it to recover the clock signal. The clean clock is fed back to provide a sampling clock to analog to digital conversion block 106. Also, the clean clock and data may be forwarded to an FEC (forward error correction) stage 110 that is optionally inserted depending on the detected signal type.

Please replace the paragraph starting on page 11, line 5 with the following:

The output of voltage controlled oscillator 202 is the clean clock signal. To lock it to the rough clock input, the clean clock is fed back through a divide by N block 204 and then to a phase detector 206. Phase detector 206 obtains a phase difference between the clean clock and the rough clock and outputs the difference to a lowpass filter 208. Lowpass filter 208 has a bandwidth of, e.g., 3-5 MHz, which sets the capture range and response time of the PLL. The output of lowpass filter 208 represents a fine adjustment to voltage controlled oscillator 202 to bring it into lock. A lock detect output from phase detector 206 indicates when voltage controlled oscillator 202 is locked to the rough clock input. It will be appreciated that the phase detection and filtering functions could be performed using a digital signal processor or other hardware. A numerically controlled oscillator could then substitute for the voltage controlled oscillator.

Please replace the paragraph starting on page 11, line 16 with the following:

Fig. 3 is a flowchart describing steps of operating transponder 100 to detect and select a received signal type employing the implementation of clock recovery block 108 that is depicted in Fig. 2A. Control processor 126 maintains a list of the possible client signal types. At step 302, control processor 126 picks a first signal type on the list. At step 304, control processor 126 configures clock recovery block 108 to attempt to lock to the selected signal type by setting the coarse input of ~~NCO 202~~ VCO 202 to match the clock rate of the selected signal type. At step 306, control processor 126 waits for a predetermined time interval for a lock indication from clock recovery block 108. The time interval may be, e.g., less than 1 millisecond. A step 308 tests whether lock was in fact achieved. If lock was not achieved, control processor 126 proceeds to step 302 to pick the next signal type on the list.

Please replace the paragraph starting on page 13, line 8 with the following:

Fig. 2C depicts an alternative structure for clock recovery block 108. In Fig. 2C, a phase frequency detector 214', in addition to performing the functions of phase frequency detector 214 in Fig. 2B, also determines the rate of the received signal by measuring a rate difference between the output of VCO 210 and a reference clock. Again, this rate is reported to control processor ~~216~~ 126.